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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Ostrow et al.

Serial No. 10/046,871

Filed: 01/15/2002

For: STATISTICALLY BASED CASCADED ANALOG-TO-DIGITAL CONVERTER CALIBRATION TECHNIQUE

Art Unit: 2819

Examiner: Wamsley, P.

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BRIEF ON APPEAL FOR APPELLANTS

Commissioner for Patents
Box 1450
Alexandria, CA

Sir:

This appeal is taken from the Office's final rejection of Claims 1-13 mailed September 5, 2003, in the subject application.

I. REAL PARTY IN INTEREST.

The real party in interest is the assignee, Raytheon Company.

II. RELATED APPEALS AND INTERFERENCES.

There are no related appeals or interferences.

III. STATUS OF ALL THE CLAIMS.

Claims 1-13 were filed with this application. During the course of prosecution before the Primary Examiner, Claims 4 and 5 were amended. Claims 1-13 in their present form appear in Appendix 1. These claims are the only claims pending in this case.

IV. STATUS OF ALL AMENDMENTS FILED SUBSEQUENT TO FINAL REJECTION.

No amendments were filed subsequent to the final rejection.

V. SUMMARY OF THE INVENTION.

The page and line numbers referred to herein are to the specification; reference characters are found in the drawing.

A method and apparatus provides calibration of an analog-to-digital converter (ADC) circuit. The ADC calibration method employs a calibration signal having symmetric or uniform probability density that is applied to the ADC input during a calibration mode. The statistics of the bit transitions at each stage in response to the calibration signal are examined. The bit transition probability density functions are computed to determine deviation from the desired "ideal" transfer function. The deviations are then minimized through the use of compensation signals applied during normal operation of the ADC. 12:5-17.

A calibration method for optimizing the transfer function of an analog-to-digital converter (ADC) [50] is recited in Claim 1. The ADC employs a cascade of n stages [10A-10C] to form a composite n-bit ADC transfer function, the ADC having an analog input [α_1] and an n-bit digital output, each stage having an analog input. The method comprises:

applying a signal having a symmetric or uniform probability density property to the ADC analog input [9:21-30];

determining at least one error value for each stage resulting from application of said signal [10:4-12:4];

using the at least one error value for each stage to compensate each of said n stages during ADC operation [8:12 - 9:2].

Claim 9 recites an analog-to-digital converter (ADC), comprising:

a cascade of N-stages [10A, 10B, 10C], wherein a first stage determines the most significant or coarse bit(s) for the ADC, and a last stage determines the least significant or finest resolution bit(s) for the ADC, the cascade of N-stages forming a composite n-bit ADC transfer function;

an ADC analog input port;

an ADC digital output port;

the first stage having a stage analog input connected to the ADC analog input port, and producing a first stage digital output and a first stage digital output;

a calibration circuit [FIG. 9: 60-68] for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input, the calibration circuit for determining at least one error value for each stage resulting from application of said signal;

an error compensation circuit [FIG. 9: k-bit trim DACs and accumulation registers] coupled to the calibration circuit for compensating each stage in response to said at least one error value for each stage.

Claim 13 recites a calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the n stages including a first stage which determines the most significant or coarse bit(s), and a last stage which determines the least significant or finest resolution bit(s), the ADC having an analog input and an n-bit digital output, each stage having an analog input. The method comprises:

applying a signal having a symmetric or uniform probability density property to the ADC analog input [9:21-30];

determining at least one error value for each stage resulting from application of said signal, by examining statistics of bit transitions at each stage to compute bit transition probability density functions for both individual stage outputs and for logical combinations of the stage outputs to determine deviation from a desired transfer function related to both gain and offset errors within and between the stages [4:24 - 5:31; 10:4-12:4];

using the at least one error value for each stage to compensate each of said n stages during ADC operation [5:11 - 7:19; 8:12 - 9:2].

VI. CONCISE STATEMENT OF THE ISSUES PRESENTED FOR REVIEW.

The issues presented on appeal are (i) whether Claims 1-13 are unpatentable over "Admitted Prior Art" ("APA") in view U.S. 4,187,466, Kasson et al. ("Kasson"), and (ii) the scope of the APA.

VII. GROUPING OF CLAIMS FOR EACH GROUND OF REJECTION WHICH APPELLANT CONTESTS.

The claims on appeal do not stand or fall together.

VIII. ARGUMENT.

A. The Requirements of 35 USC §103.

Graham v. John Deere, 383 U.S. 1, 148 USPQ 459 (1966), sets out several factual inquiries to be answered in applying Section 103, including (a) determining the scope and contents of the prior art, and (b) ascertaining the differences between the prior art and the claims at issue. In this case, this inquiry includes determining the scope of the APA.

35 USC §103 requires that the invention as a whole must be considered in obviousness determinations. The invention as a whole embraces the structure, its properties and the problem it solves. In re Wright, 6 USPQ2d 1959, 1961 (Fed.Cir. 1988).

In order to provide a basis for obviousness, the applied references must be related to the subject matter of the invention in issue and must suggest (expressly or by implication) the combination of the invention in issue. In re Sernaker, 702 F.2d 989 (Fed.Cir. 1983).

Further, the combined teachings of the prior art references should suggest the advantage of combining the teachings. In re Sernaker, supra, at 995-996.

In determining the combined teachings of the applied references, the subject matter of the claimed invention must not be utilized to provide hindsight reconstruction of the applied references. As stated by the Court of Customs and Patent Appeals In re Shuman, 361 F.2d 1008 (CCPA 1966):

> It is impermissible to first ascertain factually what appellant did and then view the prior art in such a manner as to select from the random facts of that art only those which may be modified and then utilized to reconstruct appellants' invention from such prior art. 361 F.2d at 1012.

The Examiner bears the burden of establishing a prima facie case of obviousness based on the prior art. "... 'This burden can be satisfied only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.' The patent applicant may then attack the Examiner's prima facie determination as improperly made out, or the applicant may present objective evidence tending to support a conclusion of nonobviousness." In re Fritch, 23 USPQ 1780, 1783 (Fed.Cir. 1992).

Appellants submit that the Primary Examiner has not established prima facie that the claimed invention would have been obvious in view of the APA as properly construed and Kasson, and that the claimed invention would have been obvious to one of ordinary skill in view of the APA, as properly construed, and Kasson.

B. A Prima Facie Case of Obviousness Has Not Been Established, and the references as properly construed do not teach or suggest the claimed invention.

For purposes of this appeal, appellants are content to stand on the differences between the claimed invention and the applied references discussed below, because these differences are sufficient to establish that a prima facie case of obviousness has not been established, and the applied references do not teach or suggest appellants' invention. Appellants do not concede, however, that other differences do not exist.

The APA.

FIG. 1 illustrates a block diagram of a core stage 10 used to form a one-bit per stage N-bit analog-to-digital converter (ADC). (3:7-8). FIG. 2 illustrates a block diagram of an overall one-bit state per stage, N-bit ADC 30. (3:30-31) The core stage 10 and N-bit ADC 30 are acknowledged as being known in the art, and FIGS. 1-2 have been labeled as "Prior Art."

The Examiner asserts that FIGS. 3A-8B are prior art, and that they should be labeled "Prior Art." Appellants have denied these allegations, and traversed the requirement for labeling these figures. Appellants have not conceded that these figures illustrate only that which is old. In fact, these figures are used to describe how and why a calibration technique in accordance with appellants' invention works.

Appellants respectfully request that the Examiner's holding that FIGS. 3A-8B constitute admitted prior art be reversed.

FIGS. 3A-3B illustrate output waveforms for the digital and analog outputs of stages 1 and 2 of FIGS. 1 and 2, for an input signal swept over the ADC full scale voltage range. See specification at 4:12-23. There is no discussion that FIGS. 3A-3B illustrate only that which is known. The discussion of the probability density function of digital output bits at 4:24 to 5:2 is not described as that which is already known. The specification states, at 5:3-5, that "the calculation of bit probability density function as described above can be used in the context of calibration of an analog-to-digital converter." Thus, these figures are used in an explanation of aspects of appellants' innovation, i.e. calibration of an ADC. The excitation of the ADC by this special signal and examination of output waveforms represents appellants' contribution, not that which was known in the art prior to the invention.

FIGS. 4A-8B are used in explanation of this calibration technique. FIGS. 4A-4B show output waveforms for the digital outputs and analog outputs of stages 1 and 2 of ADC 30 (FIG. 2) for an ideal probability density function, i.e. 0.5 for each stage and for an input signal which is linearly swept from Vn to Vp. (5:3-14).

FIG. 5 illustrates a simple error case where the comparator (C1) of the first stage of the ADC 30 of FIG. 2 has an offset error, in response to the input signal which is linearly swept from Vn to Vp. Both the ideal waveform (no offset error) and the error waveform is illustrated. The specification notes that "an offset

correction signal can be applied at the analog input of stage #1 and the PDF of bit #1 reexamined until a PDF of equal "1" and "0" states is obtained thus correcting for the offset error by examining only the digital output of stage #1." (5:27-31) This statement is not a statement of a property of the known ADC, but a statement of how the ADC can be corrected for an error (in accordance with appellants' innovation).

FIGS. 6A-6B, 7A-7B and 8A-8B are each described as illustrating different error conditions of the ADC of FIG. 2, and how each can be corrected. (6:1 to 7:19) These corrections are not described as techniques which are known in the art. The description of these corrections is illustrative of solution of the problem by appellants.

FIG. 9 is an exemplary hardware implementation of an N-bit ADC embodying aspects of the invention, which implements the techniques described with respect to FIGS. 3A-8B.

The final rejection states at page 4, first paragraph, that "no new features are disclosed in any of the drawings described above," i.e. FIGS. 3A-8B. Appellants have demonstrated that this is not the case, and that new features are disclosed, i.e. the probability density function in response to an ideal signal linearly swept over the input range. Moreover, the description of these figures demonstrates how errors in respective components of the ADC can be corrected, in accordance with appellants' innovations.

The final rejection further states at page 4, first paragraph, that the "ADC [50] depicted in Figure 9 is not linked to any of these figures," i.e. FIGS. 3A-8B. This statement is incorrect. The embodiment of FIG. 9 uses the same core stage (10) as depicted in FIG. 1 for each stage of the ADC 50, i.e. 10A, 10B, 10C. The specification states, at 8:12-13, that "operation of the core stages 10A, 10B, 10C is as described above regarding stage 10 of FIG. 1."

The final rejection further states at page 4, second paragraph, that the material "linked" to conventional ADC 30 clearly qualifies as prior art. No support is given for this conclusion. This paragraph further states "Applicant has provided no evidence that the exemplary embodiment [ADC 50], depicted in Figure 9, is illustrated in any other drawing," and "Lacking such evidence, the examiner must conclude that Figures 3A-8B are readable on ADC 30, as clearly stated in the current specification." These statements are in error. To the extent that FIGS. 3A-8B and accompanying description illustrate techniques for correction

of offset errors in an ADC circuit, these figures do not constitute a description of, nor is there any admission of, prior art. Rather, as explained above, these figures are used to describe correction techniques in accordance with appellants' invention, and which are carried out by the exemplary embodiment of FIG. 9. Moreover, the embodiment of FIG. 9 is linked to FIGS. 3A-8B, e.g. at 5:3-5, 5:27-31, 6:11-16, 6:27-32 and 7:14-19.

The proper scope of the APA is limited to the core stage 10 illustrated in FIG. 1, as well as connection of the core stage 10 in a multi-bit ADC as shown in FIG. 2. The response of the circuit to particularly chosen excitation signals, both ideally and with exemplary offset errors, and the recognition that errors can be corrected by application of particular correction signals is not APA. The Examiner's determination of the APA scope and content should therefore be reversed.

Claim 1

Claims 1-13 stand rejected as being unpatentable over the "Admitted Prior Art" (APA) in view of Kasson et al. (Kasson). The rejection is respectfully traversed, on the grounds that a prima facie case of obviousness has not been established, and the applied prior art as properly construed does not teach or suggest appellants' invention.

FIGS. 1 and 2 of applicants' specification show known ADC circuits, and are labeled with the legend "Prior Art." Applicants have never stated that FIGS. 3A-8B illustrate the prior art, and have denied that this is so. The analyses of bit statistics of FIGS. 4A-8B are clearly not discussed as being known in the art.

The Examiner states that "APA provides a calibration method comprising the steps of applying an input signal to an analog to digital converter, hereafter ADC; determining at least one error value; and using that value for each stage for compensation." Appellants deny that the APA provides such a calibration method, and note that the Examiner has not pointed to a calibration method in the APA. In fact, no known calibration method is described in applicants' specification for the ADC circuits shown in FIGS. 1 and 2. Even assuming without conceding that FIGS. 3A-8B are prior art, these figures also do not show such a calibration method as recited in Claim 1.

The Examiner further states that ADC provides an ADC comprising a cascade of N stages; an ADC analog input port; and ADC digital output port; a calibration circuit; and an error compensation circuit. Applicants respectfully disagree, and deny that the APA provides an ADC comprising such circuits. The circuits of FIGS. 1 and 2 do not include a calibration circuit or an error compensation circuit.

The Examiner concedes that the APA does not "teach application of a signal having a symmetric or uniform probability density." Kasson is cited as allegedly showing injection of a controlled signal in the form of a symmetric triangle wave. The Examiner alleges that it would have been obvious to have applied Kasson's teachings to APA, on the rationale that one of ordinary skill in the art would have been motivated to use a symmetric triangle wave to reduce channel crosstalk and quantizing error noise, as suggested by Kasson on column 3. Applicants respectfully disagree.

Kasson describes a technique for adding and subsequently subtracting a deterministic dither signal in the context of a digital transmission system. Kasson does not teach or suggest a method for calibrating an ADC. Rather, Kasson adds and subsequently subtracts via filtering a small deterministic dither signal whose purpose is to improve the signal-to-noise ratio of the overall system when the analog input signal is of very small amplitude, for example, a few Least Significant Bits or LSBs, relative to the full scale dynamic range of the system. The controlled signal of Kasson is applied during normal operation of the system, not during a calibration method. Kasson does not determine an error value for each stage of the ADC resulting from application of a signal having a symmetric or uniform probability density property to the ADC analog input.

Claim 1 is drawn to a calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

[A] applying a signal having a symmetric or uniform probability density property to the ADC analog input;

[B] determining at least one error value for each stage resulting from application of said signal;

[C] using the at least one error value for each stage to compensate each of said n stages during ADC operation.

The reference characters [A], [B] and [C] have been added for convenience in reference.

The APA of FIGS. 1-2 does not teach or suggest any of paragraphs A, B or C of Claim 1. Even assuming without conceding that FIGS. 3A-8B are prior art, these do not illustrate at least limitation C.

Kasson does not teach at least the features of paragraphs B and C of Claim 1.

There is in any event no suggestion or motivation to combine the APA of FIGS. 1-2 with Kasson to arrive at the invention of Claim 1. Even if the signal of Kasson is fed into the ADC of FIG. 1, the claimed invention still does not result.

The rejection of Claim 1 and the claims depending therefrom should be reversed.

Claims 2-3

Claim 2 depends from Claim 1, and further recites that the n stages include a first stage which determines the most significant or coarse bit(s), a last stage which determines the least significant or finest resolution bit(s), and wherein any intermediate stages in between the first stage and the last stage, if any, determine the intermediate bit(s). Claim 3 depends from Claim 2, and further recites that the step of determining at least one error value for each stage includes:

examining statistics of bit transitions at each stage individually as a result of application of said signal.

The Examiner states, regarding Claim 3 (and 13), that APA examines statistics of bit transitions. Appellants respectfully disagree that the APA includes this feature. The description of examination of statistics of bit transitions in the application was in the context of describing appellants' invention, not the APA of FIGS. 1-2. Moreover, even assuming without conceding that the APA has the scope asserted by the Examiner, there is no description in the APA

of examining statistics of bit transitions at each stage individually as a result of application of the said signal.

Claim 4

Claim 4 depends from Claim 3, and is allowable for the reasons discussed above regarding Claim 3. Claim 4 further recites that "said examining statistics of bit transitions includes:

> computing bit transition probability density functions for each stage output."

The Examiner asserts that the APA computes probability density functions. Appellants respectfully deny that the APA provides this teaching. The description of the calculation of bit probability density function, e.g. at 5:3, pertains to appellants' innovation, not a description of that which is known.

Claim 5

Claim 5 depends from Claim 4, and is allowable for the reasons discussed above regarding Claim 4. Claim 5 recites that said examining statistics of bit transitions includes:

> computing the bit transition probability density functions for individual bits of each stage output and for logical combinations of said individual bits of each stage output to determine deviation from a desired ideal transfer function related to both gain and offset errors within and between the stages.

The Examiner alleges, regarding Claim 5, that APA determines deviation from an ideal transfer function, thereby correcting gain and offset errors. The discussion of deviation from an ideal transfer function concerns appellants' innovations, and is not encompassed within the properly construed APA. Moreover, even assuming without conceding that the APA has the scope asserted by the Examiner, there is no description in the APA of computing the bit transition probability density functions for individual bits of each stage output and for logical combinations of the individual bits of each stage output to determine deviation from a desired ideal transfer function related to both gain and offset errors within and between the stages. The rejection does not meet the claim limitations.

Claim 6

Claim 6 depends from Claim 5, and is allowable for the reasons discussed above regarding Claim 5. Claim 6 recites that "said determining at least one error value for each stage includes using said deviation to determine said at least one error value."

The Examiner asserts that the APA uses the deviation to determine error values. Applicants deny that APA includes these features. The final rejection provides no citation to the APA to support this contention.

Claim 7

Claim 7 depends from Claim 1, and is allowable for the reasons discussed above regarding Claim 1. Claim 7 recites that said step of using said at least one error values includes, for each stage:

summing one of said at least one error values with said analog input to provide an error-compensated analog input to the stage.

The Examiner alleges that the APA adds error values to the analog input signal, but otherwise does not address the limitations of this claim. Discussions of application of an offset correction signal regarding FIGS. 3A-8B are in the context of appellants' innovations, not a discussion of what is conceded to be prior art. Moreover, even in the discussion of FIGS. 3A-8B at 4:11 to 7:19, there is no description of summing an error value with the analog input.

Claim 8

Claim 8 depends from Claim 1, and further recites that at least one of said n stages further has a reference analog input, and wherein said step of using said at least one error value for said at least one of said n stages includes:

summing one of said at least one error with said reference analog input to provide an error-compensated reference analog input.

The Examiner asserts that the APA adds an error value to a reference analog signal, but otherwise does not address the limitations of Claim 8. Discussions of application of an offset correction signal regarding FIGS. 3A-8B are in the context of appellants' innovations, not a discussion of what is conceded to be prior art.

Moreover, even in the discussion of FIGS. 3A-8B at 4:11 to 7:19, there is no description of summing an error value with the reference analog input.

Claim 9

Claim 9 is drawn to an analog-to-digital converter (ADC), comprising:

a cascade of N-stages, wherein a first stage determines the most significant or coarse bit(s) for the ADC, and a last stage determines the least significant or finest resolution bit(s) for the ADC, the cascade of N-stages forming a composite n-bit ADC transfer function;

an ADC analog input port;

an ADC digital output port;

the first stage having a stage analog input connected to the ADC analog input port, and producing a first stage digital output and a first stage digital output;

a calibration circuit for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input, the calibration circuit for determining at least one error value for each stage resulting from application of said signal;

an error compensation circuit coupled to the calibration circuit for compensating each stage in response to said at least one error value for each stage.

The APA of FIGS. 1 and 2 does not describe or teach a calibration circuit or an error compensation circuit as recited in Claim 9. Even assuming without conceding that the APA includes FIGS. 3A-8B, there is no calibration circuit or error compensation circuit disclosed therein.

Kasson does not teach or suggest a calibration circuit for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input, which determines at least one error value for each stage resulting from application of the signal. Nor does Kasson teach or suggest an error compensation circuit coupled to a calibration circuit for compensating each state in response to the at least one error value for each stage.

Because the APA and Kasson alone or in combination do not teach or suggest all claim limitations, the rejection of Claim 9 as well as the rejection of the claims depending therefrom should be withdrawn.

Claim 10

Claim 10 depends from Claim 9, and is allowable for the reasons discussed above regarding Claim 9. Claim 9 recites that the calibration circuit is adapted to determine a bit transition probability density function for each of said stage digital outputs and for logical combinations of said digital outputs to determine deviation from a desired ideal transfer function related to both gain and offset errors within and between the stages.

The Examiner asserts that the APA computes probability density functions. Appellants respectfully deny that the APA provides this teaching. The description of the calculation of bit probability density function, e.g. at 5:3, pertains to appellants' innovation, not a description of that which is known.

Claim 11

Claim 11 depends from Claim 9, and is allowable for the reasons discussed above regarding Claim 9. Claim 11 recites that each stage includes a summer circuit for summing the stage analog input with an analog error value for the stage.

The Examiner asserts that the APA adds error signals to the analog input signal, but otherwise does not address the limitations of this claim. Discussions of application of an offset correction signal regarding FIGS. 3A-8B are in the context of appellants' innovations, not a discussion of what is conceded to be prior art. Moreover, even in the discussion of FIGS. 3A-8B at 4:11 to 7:19, there is no description of a summer circuit for summing the stage analog input with an analog error value.

Claim 12

Claim 12 depends from Claim 11, and is allowable for the reasons discussed above regarding Claim 11. Claim 12 recites that at least one of the N-stages has a stage analog reference signal, and each stage further includes a reference summer circuit for summing the stage analog reference signal with an analog reference error signal.

The Examiner asserts that the APA adds error values to a reference analog signal, but otherwise does not address the limitations of this claim. Discussions of application of an offset correction signal regarding FIGS. 3A-8B are in the context of appellants' innovations, not a discussion of what is conceded to be prior art. Moreover, even in the discussion of FIGS. 3A-8B at 4:11 to 7:19, there is no description of a reference summer circuit for summing the stage analog reference signal with an analog reference error signal.

Claim 13

Claim 13 is drawn to a calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the n stages including a first stage which determines the most significant or coarse bit(s), and a last stage which determines the least significant or finest resolution bit(s), the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

[A] applying a signal having a symmetric or uniform probability density property to the ADC analog input;

[B] determining at least one error value for each stage resulting from application of said signal, by examining statistics of bit transitions at each stage to compute bit transition probability density functions for both individual stage outputs and for logical combinations of the stage outputs to determine deviation from a desired transfer function related to both gain and offset errors within and between the stages;

[C] using the at least one error value for each stage to compensate each of said n stages during ADC operation.

The APA of FIGS. 1-2 does not describe or suggest any of the limitations of Claim 13. Kasson does not teach or suggest at least the limitations of paragraphs B and C of Claim 13. For these reasons, as well as the reasons discussed above regarding Claim 1, the invention of Claim 13 is not taught or suggested by the APA or Kasson, alone or in combination.

VII. SUMMARY

The rejections under 35 USC § 103 and the holdings as to the scope and context of the APA must be reversed. The Examiner has improperly determined the scope of the prior art. A prima facie case of obviousness has not been made, and the prior art does not teach or suggest the claimed invention.

Respectfully submitted,

Leonard A. Alkov

Dated: January 7, , 2004

Leonard A. Alkov
Registration No. 30,021

Raytheon Company
P.O. Box 902 (E4/N119)
El Segundo, CA 90245-0902
Telephone: (310) 647-2577
Facsimile: (310) 647-2616

APPENDIX I

1. (Originally Presented) A calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

applying a signal having a symmetric or uniform probability density property to the ADC analog input;

determining at least one error value for each stage resulting from application of said signal;

using the at least one error value for each stage to compensate each of said n stages during ADC operation.

2. (Originally Presented) The method of Claim 1, wherein the n stages include a first stage which determines the most significant or coarse bit(s), a last stage which determines the least significant or finest resolution bit(s), and wherein any intermediate stages in between the first stage and the last stage, if any, determine the intermediate bit(s).

3. (Originally Presented) The method of Claim 2, wherein the step of determining at least one error value for each stage includes:

examining statistics of bit transitions at each stage individually as a result of application of said signal.

4. (Amended) The method of Claim 3, wherein said examining statistics of bit transitions includes:

computing bit transition probability density functions for each stage output.

5. (Amended) The method of Claim 4, wherein said examining statistics of bit transitions includes:

computing the bit transition probability density functions for individual bits of each stage output and for logical combinations of said individual bits of each stage output to determine deviation from a desired ideal transfer function related to both gain and offset errors within and between the stages.

6. (Originally Presented) The method of Claim 5, wherein said determining at least one error value for each stage includes using said deviation to determine said at least one error value.

7. (Originally Presented) The method of Claim 1, wherein said step of using said at least one error values includes, for each stage:

summing one of said at least one error values with said analog input to provide an error-compensated analog input to the stage.

8. (Originally Presented) The method of Claim 1, wherein at least one of said n stages further has a reference analog input, and wherein said step of using said at least one error value for said at least one of said n stages includes:

summing one of said at least one error with said reference analog input to provide an error-compensated reference analog input.

9. (Originally Presented) An analog-to-digital converter (ADC), comprising:

a cascade of N-stages, wherein a first stage determines the most significant or coarse bit(s) for the ADC, and a last stage determines the least significant or finest resolution bit(s) for the ADC, the cascade of N-stages forming a composite n-bit ADC transfer function;

an ADC analog input port;

an ADC digital output port;

the first stage having a stage analog input connected to the ADC analog input port, and producing a first stage digital output and a first stage digital output;

a calibration circuit for optimizing the ADC transfer function in response to application to the ADC of a calibration signal having a symmetric or uniform probability density property to the ADC analog input, the calibration circuit for determining at least one error value for each stage resulting from application of said signal;

an error compensation circuit coupled to the calibration circuit for compensating each stage in response to said at least one error value for each stage.

10. (Originally Presented) The ADC of Claim 9, wherein the calibration circuit is adapted to determine a bit transition probability density function for each

of said stage digital outputs and for logical combinations of said digital outputs to determine deviation from a desired ideal transfer function related to both gain and offset errors within and between the stages.

11. (Originally Presented) The ADC of Claim 9, wherein each stage includes a summer circuit for summing the stage analog input with an analog error value for the stage.

12. (Originally Presented) The ADC of Claim 11, wherein at least one of the N-stages has a stage analog reference signal, and each stage further includes a reference summer circuit for summing the stage analog reference signal with an analog reference error signal.

13. (Originally Presented) A calibration method for optimizing the transfer function of analog-to-digital converter (ADC) employing a cascade of n stages to form a composite n-bit ADC transfer function, the n stages including a first stage which determines the most significant or coarse bit(s), and a last stage which determines the least significant or finest resolution bit(s), the ADC having an analog input and an n-bit digital output, each stage having an analog input, the method comprising:

applying a signal having a symmetric or uniform probability density property to the ADC analog input;

determining at least one error value for each stage resulting from application of said signal, by examining statistics of bit transitions at each stage to compute bit transition probability density functions for both individual stage outputs and for logical combinations of the stage outputs to determine deviation from a desired transfer function related to both gain and offset errors within and between the stages;

using the at least one error value for each stage to compensate each of said n stages during ADC operation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	Art Unit: 2819
Ostrow et al.	Examiner: Wamsley, P.
Serial No. 10/046,871	
Filed: 01/15/2002	
For: STATISTICALLY BASED CASCADED ANALOG-TO-DIGITAL CONVERTER CALIBRATION TECHNIQUE	

BRIEF ON APPEAL FOR APPELLANTS

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST 1

II. RELATED APPEALS AND INTERFERENCES 1

III. STATUS OF ALL THE CLAIMS 1

IV. STATUS OF ALL AMENDMENTS FILED SUBSEQUENT TO FINAL REJECTION 2

V. SUMMARY OF THE INVENTION 2

VI. CONCISE STATEMENT OF THE ISSUES PRESENTED FOR REVIEW. 4

VII. GROUPING OF CLAIMS FOR EACH GROUND OF REJECTION WHICH APPELLANT CONTESTS 4

VIII. ARGUMENT 4

A. The Requirements of 35 USC §103 4

B. A Prima Facie Case of Obviousness Has Not Been Established, and the references as properly construed do not teach or suggest the claimed invention 5

The APA 6
Claim 1 8
Claims 2-3 10
Claim 4 11
Claim 5 11
Claim 6. 12
Claim 7 12
Claim 8 12
Claim 9 13
Claim 10 14
Claim 11 14
Claim 12 14
Claim 13 15

VII. SUMMARY 16

APPENDIX I 17

TABLE OF AUTHORITIES

Graham v. John Deere, 383 U.S. 1, 148 USPQ 459 (1966) 4

35 USC § 103 4

In re Wright, 6 USPQ 2d 1959, 1961 (Fed.Cir. 1988) 4

In re Sernaker, 702 F.2d 989 (Fed.Cir. 1983). 4

In re Sernaker, supra, at 995-996 4

In re Shuman, 361 F.2d 1008 (CCPA 1966) 4

In re Fritch, 23 USPQ 1780, 1783 (Fed.Cir. 1992) 5